Indian J. Phys. **71A** (3), 323–328 (1997)

IJP A
- an international journal

Electrical parameters of CdSe-Nd_2O_3 and GaAs-Nd_2O_3 Thin-Film Transistors

M Puzari

Department of Physics, North Lakhimpur College,
North Lakhimpur-787 001, Assam, India

and

B Baishya

Department of Physics, Dibrugarh University,
Dibrugarh-786 004, Assam, India

Abstract : Nd_2O_3 has been used as gate insulator in CdSe and GaAs thin film transistors (TFTs) fabricated in staggered electrode structure by multiple pump down (MPD) method of vacuum evaporation. The d.c. characteristics of the devices are presented and some electrical parameters are calculated from the I-V characteristics and the theoretical model proposed by Levinson *et al.*

Keywords : Neodymium oxide, Thin-Film transistor

PACS Nos. : 73.61.r ; 73.90.f ; 81.60.cp

1. Introduction

The TFTs are of current interest for their suitability in large area circuits. The choice of semiconductor-insulator combination plays a key role in realizing the ultimate properties of TFT [1], vacuum evaporated Nd_2O_3 films [2] having chemical and mechanical stability, high breakdown field strength (1.5×10^6 V cm^{-1}), low dissipation factor (≈.0045) and high dielectric constant (12.64) fulfil the requirements of good insulator stated by earlier workers [1,3]. TFTs with CdSe active layer are reported to be stable, reproducible and capable of withstanding high voltage and they are widely used for addressing in flat panel liquid crystal

displays [4–7]. GaAs, a high band gap III-V compound which performs well in MESFET and high speed devices is also tested as TFT semiconductor.

2. Experimental details

TFTs have been fabricated by MPD method on chemically and ultrasonically cleaned glass substrates by vacuum deposition of different layers in the given sequence : aluminium source drain electrode, semiconductor (CdSe or GaAs) at elevated substrate temperature (175°C for CdSe 150°C for GaAs), Nd_2O_3 and finally an aluminium gate electrode. Various geometrical patterns were obtained with the help of mechanical masks. The channel was defined by a 50 μm wire grill fixed on the source-drain mask. All the depositions were made in vacuum of the order of 10^{-6} torr. Film thickness was measured by multiple beam interference method. The fabricated samples were annealed in air at 200°C for 3-4 hours and then, stored in clean desiccator for 20-25 days to obtain the saturated characteristics.

3. Results and discussion

The drain current I_D vs drain voltage V_D characteristics for CdSe-Nd_2O_3 and GaAs-Nd_2O_3 TFTs are shown in Figures 1 and 2 respectively.

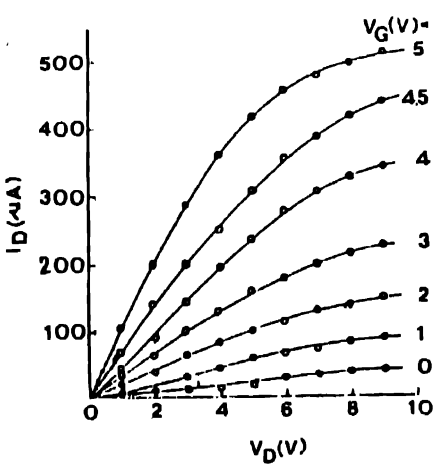

Figure 1. Source drain characteristics of CdSe-Nd_2O_3 TFT.

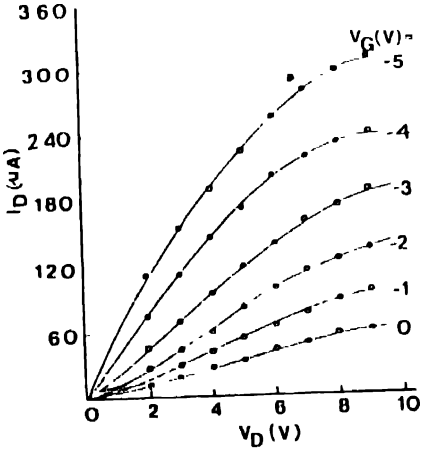

Figure 2. Source drain characteristics GaAs-Nd_2O_3 TFT.

The field-effect characteristics of CdSe (curve 'a', scale 'A') and GaAs (curve 'b', scale 'B') TFTs at V_D = 8 V are shown in Figure 3. The pinch-off voltage for CdSe and GaAs TFTs, noted from Figure 3 are −1.4 V and +2.3 V respectively.

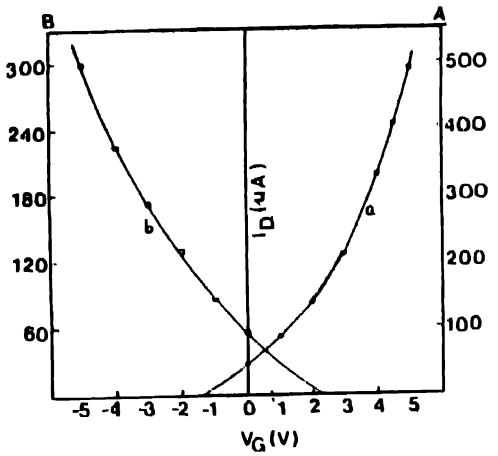

Figure 3. Field-effect characteristics of $CdSe$-Nd_2O_3 (curve 'a' scale 'A') and GaAs-Nd_2O_3 (curve 'b' scale 'B') TFTs.

Various transistor parameters, such as transconductance (g_m) output resistance (r_d), amplification factor (μ) and gain-band width product as calculated from the characteristics are presented in Table 1.

Table 1.

Device type	Trans conductance g_m (μmho)	Output resistance r_d (Kohm)	amplification factor (μ)	Gain-banwidth product (KHz)
$CdSe$-Nd_2O_3	225	80	18	26.7
GaAs-Nd_2O_3	100	111	11.1	8.85

Due to the polycrystalline nature of the CdSe and GaAs films, the existence of traps in the devices is most common. Hence the grain boundary trapping model [8] may be used to characterize the TFTs. According to this model the drain current I_D of a TFT with polycrystalline material is given by

$$I_D = w\mu_b(V_D / l)C_i V_G \exp(-q^3 N_t^2 t / 8\varepsilon KTC_i) \quad (1)$$

where w and l are the channel width and length, μ_b is the mobility, C_i is the insulator capacitance per unit area, N_t is the trap concentration per unit area and t is the thickness of the semiconductor film.

It is evident from equation (1) that the plot of ln (I_D/V_G) as a function of $1/V_G$ is a straight line (Figure 4) from the slope of which N_t can be obtained. From the pre-exponential part of equation (1) the value of mobility can be estimated.

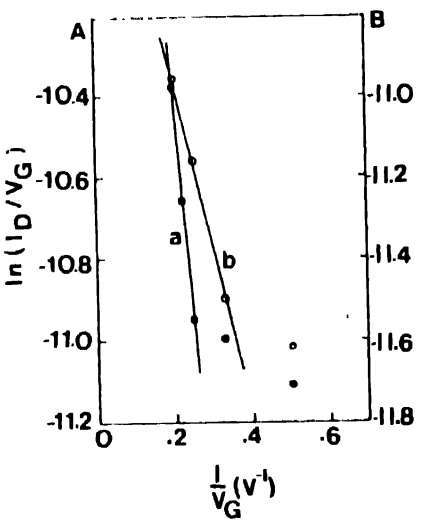

Figure 4. Plots of ln(I_D/V_G) for CdSe-Nd_2O_3 (line 'a' scale 'A') and GaAs-Nd_2O_3 (line 'b' scale 'B') TFTs.

Further departure from linearity in Figure 4 would occur when

$$N_G/t = N_D^*$$

where $N_G = (C_i/q)\ V_G$ and N_D^* is the critical donor density. The crystal size 'L' can be estimated from $N_D^* = N_t/L$. The value of different parameters obtained for the present devices are listed in Table 2.

Table 2.

Device type	Trap density N_t ($\times 10^{12}$ cm^{-2})	Critical donor density N^*_D ($\times 10^{18}$ cm^{-2})	Grain size L (Å)	Mobility μ_b (cm^2 v^{-1} s^{-1})
$CdSe$-Nd_2O_3	3.08	2.48	124	3.14
$GaAs$-Nd_2O_3	2.44	2.28	107	0.365

The reported TFT performances are affected by drift phenomena. After the application of gate bias, charge carriers are trapped by the fast states in the semiconductor layer and by the slow states at the interface with the gate oxide [1]. These trapped carriers screen the gate field and consequently the TFT ON current decreases with time whereas the OFF current increases with time due to the generated free electrons [7]. Though some important parameters for CdSe TFTs are found better than those for GaAs TFTs, the mobility estimated is not adequate. This is attributed to the increased surface scattering due to introduction of surface states by atmospheric contamination during exposure of the semiconductor layer prior to the deposition of the oxide film [9,10]. The semiconductor-insulator interface dominate the TFT characteristics, in spite of the presence of grain boundaries [11]. Periodic record of the I-V data revealed that devices of both types deteriorated with time. However, the rate of deterioration was found slower in CdSe TFTs.

4. Conclusion

TFTs obtained with the semiconductor-insulator combination of $CdSe$-Nd_2O_3 and $GaAs$-Nd_2O_3 showed good channel modulation. The characteristics of CdSe TFTs were better than the GaAs TFTs. The mobility and transconductance obtained and stability observed, needed further improvement for circuit applications.

Acknowledgment

One of the authors (M.P.) is thankful to University Grants Commission and North Lakhimpur College authority for providing financial support.

References

[1] J C Anderson *Thin Solid Films* **36** 299 (1976)

[2] V S Dharmadhikari and A Goswami *Thin Solid Films* **87** 199 (1982)

[3] A Van Calster and A D Vos *Electrocomp. Sci. Technol.* **6** 131 (1980)

[4] T P Brody *IEEE Trans.* **ED31** 1614 (1984)

[5] M J Lee, C P Judge and S W Wright *IEEE Trans.* **ED39** 2664 (1992)

[6] J De Baets, J Vanfleteren, I D Rycke, J Doutreloigne, A Van Calster and P D Visschere *IEEE Trans.* **ED37** 636 (1990)

[7] G Moersch, P Rava, F Schwarz and A Paccagnella *IEEE Trans.* **ED36** 449 (1989)

[8] J Levinson, F R Shepherd, P J Scanion, W D Westwood, G Este and M Rider *J. Appl. Phys.* **53** 1193 (1982)

[9] P K Deka and B Baishya *Thin Solid Films* **112** L5 (1984)

[10] P Singh and B Baishya *Thin Solid Films* **147** 25 (1987)

[11] J C Anderson *Thin Solid Films* **38** 151 (1976)